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We Claim:

1. A method of fabricating a closed-form Josephson junction comprising:

forming an interior of a closed-form shape in a trilayer chip, wherein said trilayer chip comprises a substrate, a first superconducting layer, an insulating layer, and a second superconducting layer;

depositing a negative photoresist on said trilayer chip;

exposing the backside of said trilayer chip with an illumination source;

removing a region of said negative photoresist that has not been exposed to said illumination source; and

etching the chip to form an exterior of said closed-form Josephson junction.

2. The method of claim 1, wherein said substrate is transparent to said illumination source and wherein at least one of said first superconducting layer, said insulating layer, and said second insulating layer block said illumination source.

3. The method of claim 2, wherein said illumination source is ultra-violet (UV) radiation.

4. The method of claim 1, wherein said substrate is sapphire.

5. The method of claim 1, wherein said first superconducting layer comprises niobium (Nb), aluminum (Al), or lead (Pb).

6. The method of claim 1, wherein said second superconducting layer comprises niobium (Nb), aluminum (Al), or lead (Pb).

7. The method of claim 1, wherein said first superconducting layer and said second superconducting layer are made of different superconducting materials.

8. The method of claim 1, wherein a thickness of the first superconducting layer and a thickness of said second superconducting layer is about 100 nm to about 300 nm.

9. The method of claim 1, wherein said insulating layer comprises aluminum-aluminum oxide (Al-AlO_X).

10. The method of claim 1, wherein a thickness of said insulating layer is about 1 nm to about 20nm.

11. The method of claim 1, the method further comprising:

baking said negative photoresist after said exposing; and

removing said exposed negative photoresist.

12. The method of claim 11, wherein the temperature of during at least a portion of said baking is about 120°C and about 160°C.

13. The method of claim 1, wherein said forming comprises ion beam etching, reactive ion etching, or electron cyclotron resonance plasma etching.

14. The method of claim 1, wherein said negative photoresist is an organic negative photoresist.

15. The method of claim 1, wherein a thickness of said negative photoresist is between about 0.2 μm and 2 μm.

16. The method of claim 1, wherein said negative photoresist comprises cross-linked polymethylmethacrylate (PMMA) that is made by exposing PMMA to an electron exposure dose.

17. The method of claim 1, wherein an average exterior width of said closed-form Josephson junction is greater than about 1μm and less than about 1000μm.

18. The method of claim 1, wherein said exposing comprises flood radiation, wherein the backside of said trilayer chip is uniformly exposed with said illumination source.

19. The method of claim 1, wherein said removing comprises developing said chip in a chemical solution.

20. The method of claim 1, wherein said etching comprises etching a region of said first superconducting layer.

21. The method of claim 1, wherein said etching comprises ion beam etching, reactive ion etching, or electron cyclotron resonance plasma etching.

22. The method of claim 1, wherein said etching includes etching said insulating layer.

23. The method of claim 22, wherein said etching includes argon (Ar) sputtering.

24. The method of claim 1, the method further comprising attaching an electrode to said second superconducting layer.

25. A method for insulating a closed-form Josephson junction, the method comprising:

depositing a layer of negative photoresist on a chip, wherein said chip includes said closed-form Josephson junction;

backside irradiating said chip; and

developing said chip to remove unexposed regions of said negative photoresist.

26. The method of claim 25, wherein said backside irradiating comprised ultraviolet flood radiation that is directed at the substrate side of said chip.

27. A method for attaching an electrode to a closed-form Josephson junction, the method comprising:

depositing a photoresist mask on a chip, wherein said chip includes at least one insulated closed-form Josephson junction;

irradiating said photoresist mask with an illumination source;

developing said chip;

fixing said photoresist mask; and

depositing a superconducting material on said chip, thereby attaching said top electrode to said closed-form Josephson junction.

28. The method of claim 27, wherein a thickness of said photoresist mask is between about 100 nm and about 500 nm.

29. The method of claim 27, wherein said irradiating comprises ultraviolet flood radiation directed at a substrate side of said chip.

30. The method of claim 27, wherein said fixing comprises electron beam exposure of said chip that forms a region of cross-linked photoresist.

31. The method of claim 30, the method further comprising developing said chip to remove a region of said photoresist that is not cross-linked.

32. The method of claim 27, wherein said exposing comprises x-ray irradiation to form a region of cross-linked photoresist.

33. The method of claim 27, wherein said photoresist mask comprises polymethylmethacrylate.

34. The method of claim 27, wherein said photoresist mask includes AZ5214E.

35. The method of claim 27, wherein said photoresist mask is exposed to a dose of about 1 milliCouries per square centimeter (mC/cm^2) with electrons having energy of about 20 kilo-electron Volts (keV).

36. A supercomputing structure comprising a closed-form Josephson junction, wherein said closed-form junction is manufactured by:

forming a closed-form shape in a trilayer chip, wherein said trilayer chip comprises a substrate, a first superconducting layer, an insulating layer, and a second superconducting layer;

depositing a negative photoresist on said trilayer chip;

exposing the backside of said trilayer chip with an illumination source;

removing a region of said negative photoresist that has not been exposed to said illumination source; and

etching the chip to form said closed-form Josephson junction.

37. The supercomputing structure wherein said closed-form junction is heart shaped.